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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Application Number: 09/376,063
Filing Date: August 17, 1999
Appellant(s): ANDOH, SEIJI

Phillip G. Avruch (Reg. No. 46,076)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/09/ appealing from the Office action mailed 03/22/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

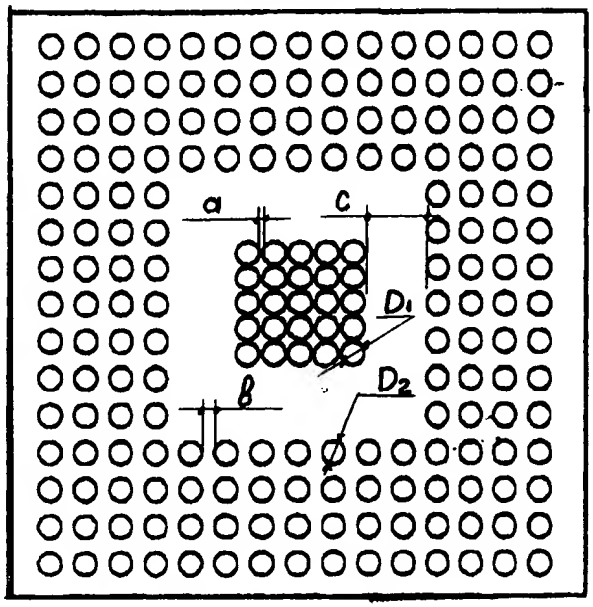
5,462,261	Bond et al	6-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

First: In order to clarify the following rejection Examiner suggests to depicture the claims of the present application as follows:

Diagram I



Wherein: N_1- is a quantity of the solder bumps in the first (central) bump unit;

N_2- is a quantity of the solder bumps in the second (peripheral) bump unit;

P_1 – a first (central area) plurality of bumps;

P_2 – a second (peripheral area) plurality of bumps;

a – is first distance [between bumps in the first (central) bump unit];

b - is a second distance [between bumps in the second (peripheral) bump unit];

c – is a third distance [between the central area bump unit and the peripheral area bump unit], or an intermediate area;

D_1 – is a diameter of a bump in the first (central) bump unit;

D_2– is a diameter of a bump in the second (peripheral) bump unit;

W – is a width of the intermediate area (claimed in claim 22 and presenting a synonym of the previously defined "c").

Second: Designate as a "CORE" a set of main structural limitations of the claims in the present application, which are claimed as:

A semiconductor device, comprising: a substrate having a main surface and a back surface, wherein said back surface has a central area, a distinct intermediate area in which no bumps are disposed, surrounding said central area, and a peripheral area surrounding said intermediate area; a semiconductor chip disposed on said main surface; a first bump unit disposed in said central area of said back surface, wherein said first bump unit includes a plurality of bumps that are disposed a first distance apart from each other, and wherein said first bump unit radiates heat from said semiconductor device; and a second bump unit formed in said peripheral area of said back surface, wherein said second bump unit includes a plurality of-bumps that are disposed a second distance apart from each other.

Third: Designate as an "ASSUMPTION" a statement in claims 26 and 28 that: "a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other sufficient to assure that upon application of a heat treatment to the device for the purpose of mounting the device to a circuit board. causing the bumps of the first and second bump units to melt, the bumps of the second bump unit remain apart from each other, ... wherein the bumps of the first bump unit are

sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body".

Therefore, using the above diagram and designations, it would be possible to present claims of the instant application as follows:

Claim 20: The CORE wherein: b > a and b < c;

Claim 22: (Depends on claim 20) The CORE, wherein: b > a and b < c; and wherein c > b (which now can be clearly understood as a duplicate of the claim 20);

Claim 24: (Depends on claim 22) The CORE, wherein: b > a and b < c; and wherein $N_2 > N_1$;

Claim 25: (Depends on claim 24) The CORE, wherein: b > a and b < c; wherein $N_2 > N_1$; and wherein P_1 and P_2 are spherical in shape (which does not make a technical sense in the claimed CORE, because it is a single solder bump, which can be claimed as being spherical in shape, rather than a plurality of bumps);

Claim 26: The CORE, wherein b > a; b < c; and the "ASSUMPTION" is added;

Claim 27: (Depends on claim 26) The CORE, wherein b > a; b < c; the "ASSUMPTION" is added; and bumps are made from solder;

Claim 28: The CORE, wherein b > a; b < c; and the "ASSUMPTION" is added; (which now can be clearly understood as duplicate of the claim 26);

Claim 29: (Depends on claim 26) The CORE, wherein b > a; b < c; the

"ASSUMPTION" is added; and bumps are made from solder; (which now can be clearly understood as duplicate of the claim 27);

Claim 31: (Depends on claim 25) The CORE, wherein: b > a and b < c; N > N ; P and P are spherical in shape; and wherein a = D x (1 to 1.4) and b = D x (1.6 to 1.7).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 20, 22, 24-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bond et al.

Bond et al teach a semiconductor device 8, Fig. 2, comprising: a substrate 14 having a main surface and a back surface, wherein said back surface has a central area, a distinct intermediate area surrounding said central area and a peripheral area surrounding said intermediate area; a semiconductor chip 10 formed on said main surface; two distinct groups of separate solder bumps 18: A first bump unit formed in the heat radiating central area having a first plurality ("P ") of bumps 18 disposed a first distance ("a") apart from each other, and a second bump unit formed in the signal peripheral area having a second plurality (P ") of bumps disposed a second distance

("b") apart from each other, wherein said first bump unit radiates heat from said semiconductor device, and said second bump unit is located in the peripheral area of the back surface distinctly apart from the first bump unit (The above represents the "CORE"). Bond et al teach furthermore said second distance ("b") being greater than said first distance ("a"); said second bump unit is greater in quantity of solder bumps that the first bump unit (N > N), and said solder bumps are spherical in shape. Regarding to the "ASSUMPTION" that because a first plurality ("P ") of bumps is disposed a first distance apart from each other sufficiently close so that upon applying heat they are would be inherently capable to melt together: First: Bond et al in teach that: "While packaged integrated circuit 8 according to this embodiment of the invention is shown in each of Figs. 1 and 2 as already attached to system circuit board 20, it is to be understood by those of ordinary skill in the art that packaged integrated circuit 8 according to this embodiment of the invention will often be individually manufactured and sold, with the purchaser performing the installation of packaged integrated circuit 8 to system circuit board 20 in a computer or other end equipment." (col. 3, lines 50-57), Second: Bond et al in Fig. 2 also teach a first plurality of bumps18 disposed touching each other, so that upon applying heat they would inherently be capable to melt together, and it is inherent that the signal bumps 18 of the second bump unit will remain apart from each other. Bond et al teach all the limitations of the claims 20, 22, 24-29 except the limitation that the second distance("b") is less than a width of the intermediate area ("c"); and Bond et al also teach all the limitations of the claim 31 except the limitations that: the second distance("b") is less than a width of the

intermediate area ("c"); the first distance being about 1 to 1.4 times the diameter ("D ") of the bumps of the first bump unit, and the second distance being about 1.6 to 1.7 times the diameter ("D ") of the bumps of the second bump unit. It would have been obvious to one skilled in the art at the time invention was made to employ in the device by Bond et al the second distance being less than a width of the intermediate area, and to make the first distance about 1 to 1.4 times the diameter of the bumps of the first bump unit, and the second distance about 1.6 to 1.7 times the diameter of the bumps of the second bump, in order to avoid shortening of signal solder bumps and enhance the heat dissipation, since such a modification would have involved a mere change in the sizes of the components or a mere change in the ranges of the distances between them. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955). Establishing of such workable ranges would also have been obvious to one having ordinary skill in the art at the time the invention was made, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Applicant has not shown that these particular sizes or ranges of sizes are critical by showing that the claimed range achieves unexpected results relative to the prior art range. (In re Woodruff, 919 F. 2d 1575, 16 USPQ2d 1934, Fed. Cir. 1990). To establish unexpected results over a claimed range, applicant should compare a sufficient number of tests both inside and outside the claimed range to show the criticality of the claimed range. (In re Hill, 128 USPQ 197 CCPA 1960).

(10) Response to Argument

Applicant argues that Examiner has not met the burden of proof in establishing that the appealed claims are obvious: Examiner respectfully disagrees: First: Applicant claims a semiconductor device having a plurality of separate solder bumps grouped distinctly in the signal peripheral area and in the heat transferring central area. It is important to note that applicant does not claim a unitary heat transferring body made of the group of solder bumps in the heat transfer area as being a part of the claimed structure. Instead the solder bumps in the heat transfer area are claimed as being placed close enough to be melted together upon application of a heat treatment. As it was written in the previous office actions, none of the other important for this technological process information, such as: type of the solder, temperature and longevity of the reflowing process has not been claimed or explained in the specification. Second: Bond et al teach a semiconductor device 8, Figs 1-6, also having two distinct groups of separate solder bumps 18: one in the signal, peripheral area and another in the heat transferring, central area. Fig. 2 clearly shows solder balls 18 located in the central, heat transfer area without any distance between them. Bond et al in also teach that: "While packaged integrated circuit 8 according to this embodiment of the invention is shown in each of Figs. 1 and 2 as already attached to system circuit board 20, it is to be understood by those of ordinary skill in the art that packaged integrated circuit 8 according to this embodiment of the invention will often be individually manufactured and sold, with the purchaser performing the installation of packaged integrated circuit 8 to system circuit board 20 in a computer or other end equipment." (col. 3, lines 50-57),

which makes it obvious to conclude that during such an installation upon applying heat solder balls in central area shown if Fig. 2 would definitely melt together. Also in Fig. 2 signal solder bumps are shown located distinctly apart from the central group of bumps. Third: Applicant assumes that: " Bond et al teaches away from the present invention by using a solder mask to keep the central solder leads separate" (page 14, lines 8-9). Examiner disagrees: Solder mask are used to place solder balls in ball-grid-array manner, even if such a ball-grid-array would comprise solder balls touching each other, as Bond et al in Fig. 2 show it. However, discussion about solder mask in Figs. 3-6 (col. 5, lines 36-50) is related to a second embodiment of the Bond et al invention (col. 5, lines 6-7), while Figs. 1-2 disclose a first embodiment of the invention and do not show any solder mask. Forth: In discussing figures of the Bond et al reference (page 16, lines 8-23) appellant disregards Fig. 2 of Bond et al as showing the semiconductor device already attached to system circuit board, lacking in detail, not to scale and contradictive to Fig.1. Examiner disagrees: a) As it was stated above, an electronic package by Bond et al may be sold separate from a circuit board and can be installed later; b) Fig. 1 is defined by Bond et al as cross-section of Fig. 2. Hence, it is Fig. 2, should be considered as a main vision of the claimed structure, rather than Fig.1, which in its turn should be declared lacking in detail, not to scale and contradictive to Fig. 2. However, lacking an explanation by Bond et al regarding differences between these two figures, examiner consider them as showing different embodiments, or at least two different ideas of a central ball-grid array, which do not contradict to each other. Fifth: Applicant assumes that: "Examiner ignores the fact, that

Bond et al fails to disclose any melting together of the solder bumps in the central area during the reflow process used to mount the semiconductor device 18 to the main circuit board". Examiner disagrees: a) Applicant has not claimed a circuit board as a distinctive part of invented structure, but rather claimed that central area solder bumps are located close enough to melt together upon application of a heat during the reflowing process when being mounting on a circuit board. As it was said above, Bond et al also disclose a semiconductor electronic package, which later could be mounted on a circuit board. The supposed "unitary body" made of melted together solder bumps in the present application is not a part of the claimed device (such as, for example, a solid solder mass 26 described and claimed as a distinctive part of the structure in the reference by Katchmar previously cited and discussed), but rather an assumption, which cannot be considered as distinguishing the invented structure over the prior art of record. Sixth: Considering that a technique to avoid a shorting between solder balls (bumps) connections during a reflow (heat applying) process by manipulating sizes of the balls and/or the distances between them is well known in the art, it would be obvious to assume that in the device by Bond et al an opposite result (melting solder balls in the central area together) could also be achieved by manipulating sizes of the central area solder balls and/or the distances between them. Seventh: examiner disagrees with applicants assumption that: "The difference between the claimed invention and the reference by Bond et al is not a matter of degree, but rather one of kind". On the contrary, both devices are substantially similar semiconductor packages having the similar structural design, wherein the difference is only a matter of degree,

consisting differences between ranges of certain relationships between diameters of solder balls and distances between groups of solder balls and between the solder balls themselves. (See discussed above "b < c" and " a = D x (1 to 1.4) and b = D x (1.6 to 1.7"). As it was said above, applicant has not shown that particular ranges of solder balls sizes or relationships between distances between them are critical by showing that the claimed range achieves unexpected results relative to the prior art range, and applicant himself admitted in the previous communication (see Remarks filed on 09/30/2003, page 2, lines 15-20) that: "...in this case, a person of ordinary skill in the art could readily determine what spacing, or range of spacing, of the bumps in the first bump unit would be sufficiently close such that the bumps would fuse into a unitary body upon application of the heat treatment ".

Based on the above examiner concludes: First: The embodiment shown by Bond et al on Fig. 2 clearly shows a structure comprising all basic structural elements of the claimed invention combined in the similar way and having the similar functions as in the present application (The above defined "CORE"). Second: In Fig. 2 of the reference by Bond et al heat radiating central group of bumps is shown having bumps touching each other, the same way central bumps 13 are shown by the Applicant in Fig. 2 of the present application. Therefore, it is inherent that solder bumps shown on Fig. 2 by Bond et al would melt in a unitary body when applying a heat in a process of mounting the semiconductor package on a circuit board, although such an assumption cannot be considered as a patentable structural limitation in an apparatus claim. Third: Applicant has not shown that claimed particular sizes or ranges of sizes are critical by showing

that the claimed range achieves unexpected results relative to the prior art range. For example, it is inherent to avoid shorting of signal bumps during a reflowing process by designing a certain distance between them, or to manipulate a distance between heat radiating central bumps and signal transmitting peripheral bumps in order to prevent excessive heat transfer to a peripheral area of a semiconductor package. Therefore, it would be obvious to one skilled in the art at the time invention was made to modify distances between groups of the signal and thermal solder bumps and between the signal solder bumps in the device by Bond et al.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Primary Examiner

Michael Datskovsky

September 28, 2005

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